

Low Voltage, Low Power VLSI Subsystems By Kiat-Seng Yeo

By Kiat-Seng Yeo

Low Low--Power VLSI Design Power VLSI Design Low Low Power VLSI Design Power VLSI Design Flip-flops are operated at full voltage and half the clock frequency. 19

<https://www.scribd.com/doc/273238399/Low-Power-VLSI-Design>

Detailing the latest techniques in low-voltage VLSI design, Yeo (electrical and electronic engineering, Nanyang Technological University, Singapore) and Roy

<http://www.amazon.it/Low-Voltage-Power-VLSI-Subsystems/dp/007143786X>

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<http://www.amazon.com/Kiat-Seng-Yeo/e/B001HQ3UD0>

Fishpond Australia, Low Voltage, Low Power VLSI Subsystems by K Roy K Yeo. Buy Books online: Low Voltage, Low Power VLSI Subsystems, 2004,

<http://www.fishpond.com.au/Books/Low-Voltage-Low-Power-VLSI-Subsystems-K-Yeo-K-Roy/9780071437868?keywords=007143786X>

2010), Low-Voltage, Low-Power VLSI Subsystems Yeo Kiat Seng and Kaushik Roy, Low-Voltage, and Yeo Kiat Seng, Low-Voltage Low-Power Digital

<http://epd.sutd.edu.sg/faculty/yeo-kiat-seng/>

Kiat-Seng Yeo is the author of Low Voltage, Low Power Vlsi Subsystems (4.29 avg rating, 14 ratings, 1 review, Kiat-Seng Yeo s Followers. None yet.

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leakage can exceed 50% of total power consumption. The reason for a growing importance of subthreshold conduction is that the supply voltage low, to maintain

http://en.wikipedia.org/wiki/Subthreshold_conduction

A 100dB SFDR 0.5V pk-pk Band-Pass DAC Implemented on a Low Voltage CMOS Process. VLSI Kiat Seng Yeo: A 1-V CMOS Ultralow-Power Very Large Scale Integration

http://dblp.l3s.de/?q=VLSI-SoC+%28Selected+Papers%29&search_opt=venuesOnlyExact&newQuery=yes&resTableName=query_resultsGnYDX&resultsPerPage=100

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CMOS VLSI Design Design for Low Power (esp. on clock), short wires VDD: lowest suitable voltage f: Reduce static power Low Power Design Reduce dynamic power a:
<http://users.ece.utexas.edu/~adnan/vlsi-05-backup/lec18LowPower.ppt>

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